Preliminary Amendment
National Stage of PCT/GB2005/000788
Attorney Docket No. Q96948

## AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

## **LISTING OF CLAIMS:**

1. (original) A non-volatile memory system comprising:

non-volatile memory divided into a polarity of segments each segment having an address in an address space,

means for copying any one segment to be reprogrammed into a first RAM, the first RAM having a size at least equal to the segment size,

a second RAM for holding a reprogrammed code,

writing means for writing the reprogrammed code from the second RAM into the at least one segment to be reprogrammed, and

control means arranged to enable execution of the programme from the first RAM during the reprogramming.

- 2. (original) The system according to claim 1, wherein the segments are substantially equal in size.
- 3. (original) The system according to claim 1 or claim 2, wherein each segment contains some unused space.
- 4. (original) The system according to any of claims 1 to 3, wherein the control means comprises internal logic components.
- 5. (original) A method of reprogramming a non-volatile solid stage memory system comprising a priority of segments each segment having an address in an address space, two RAMs each at least equal in size to a single memory segment, and control means capable of

Preliminary Amendment National Stage of PCT/GB2005/000788 Attorney Docket No. Q96948

enabling the execution of the program from the first RAM during reprogramming, the method comprising steps of:

copying at least one segment to be reprogrammed into the first RAM diverting programme execution to the first RAM, holding a reprogrammed code in the second RAM, writing the reprogrammed code from the second RAM into the at least one segment to be reprogrammed, and

reverting to the original address instructions for the segment.

6. (currently amended) A user interface for guiding a user through a reprogramming of a non-volatile solid state memory system comprising a polarity of segments each segment having an address in an address space, two RAMs each at least equal in size to a single memory segment, and control means capable of enabling the execution of the programme from the first RAM during the reprogramming, the user interface comprising:

a graphical representation of the imbedded processor showing the contents of each segment,

means for selecting the segment to be reprogrammed, and means of initiating the method of reprogramming according to claim 5 any one of claims 5 to 7.